Remarks

The present Request for Continued Examination (RCE) and amendment are filed in response to the final Office Action mailed July 25, 2007. Claims 1-14 and 20-29 are pending in the application.

In the Office Action, claims 23-24 were rejected under 35 U.S.C. § 112, paragraph 2 as being indefinite. In particular, the Examiner noted that Claims 24 and 25 recite a simulation while Claim 23 recites an etch simulation. Applicants have amended Claims 24 and 25 to refer to the etch simulation. Similar changes have been made in Claims 3, 4, 6, 7, 10, 11, 13, 14, 21, and 22. In light of the amendments it is requested that the Examiner withdraw the § 112 rejection.

Claims 1-14 and 20-33 were also rejected as being anticipated by Kim et al. U.S. Patent No. 6.544,699. Applicants respectfully traverse the rejection. The Kim reference cited by the Examiner discloses a technique for improving model-based OPC by determining the best focus and dose conditions. The references says that numerical models for the lithographic imaging and semiconductor process simulation have significantly improved in both accuracy and speed and can be integrated with an interactive OPC technique. See Col. 2, lines 60-65. However, nothing in the '699 patent teaches or suggests a method of compensating mask/reticle data for lithographic process distortion that performs an etch simulation of a set of mask/reticle data, using the results of the etch simulation to produce a revised set of mask/reticle data that are compensated for etch effects and performing OPC to produce a set of OPC-corrected mask/reticle data that compensates for optical/resist process distortions using the revised set of mask/reticle data as a target layer for the OPC as set forth in Claims 1, 8 and 20.

As described on page 5, lines 1-21 of the application, one embodiment of the invention first performs an etch simulation and then uses the etch-compensated data produced from the etch simulation as the target layer for the OPC process. OPC corrections are made until the simulated

layout matches the new etch-compensated target layer. Nothing in the prior art cited by the Examiner suggests that an etch simulation of a target layout should be performed prior to performing OPC and that the results of the etch simulation should be used to produce a new target layer for the OPC analysis. Because the Kim et al. patent does not disclose the combination of method steps recited in Claims 1, 8 and 20 it is submitted that these claims and the claims that depend thereon are allowable.

With respect to Claims 5, 12 and 23 it is submitted that Kim et al. does not disclose reading an initial set of mask/reticle data; performing an etch simulation of etch effects that would occur if a wafer is exposed using a mask/reticle corresponding to the initial set of mask/reticle data; calculating etch biases from the results of the etch simulation and applying the etch biases that are calculated from the initial set of mask/reticle data within a model-based optical process correction loop.

As set forth on page 6 of the application, using the previously calculated etch biases within an OPC loop speeds processing. Because the Kim et al. references do not disclose the combination of method steps recited in Claims 5, 12 and 23, it is submitted that these claims and the claims that depend thereon are allowable.

In light of the above, it is submitted that all pending claims are in condition for allowance. It is therefore requested that the Examiner withdrawn the rejections and pass this application to issue.

If the Examiner has any additional questions regarding the application, the Examiner is invited to call the undersigned at the number listed below.

Respectfully submitted,

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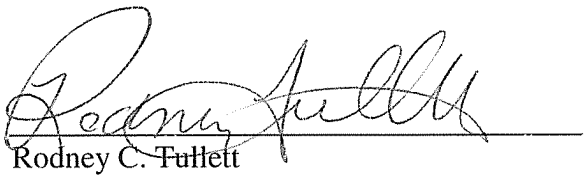
By 
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